

P65U V10

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32  
Tall DVI-D + HDMI+ DP


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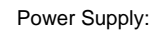
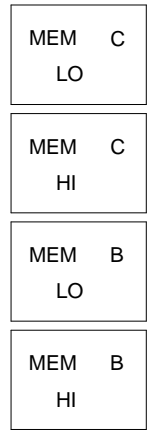



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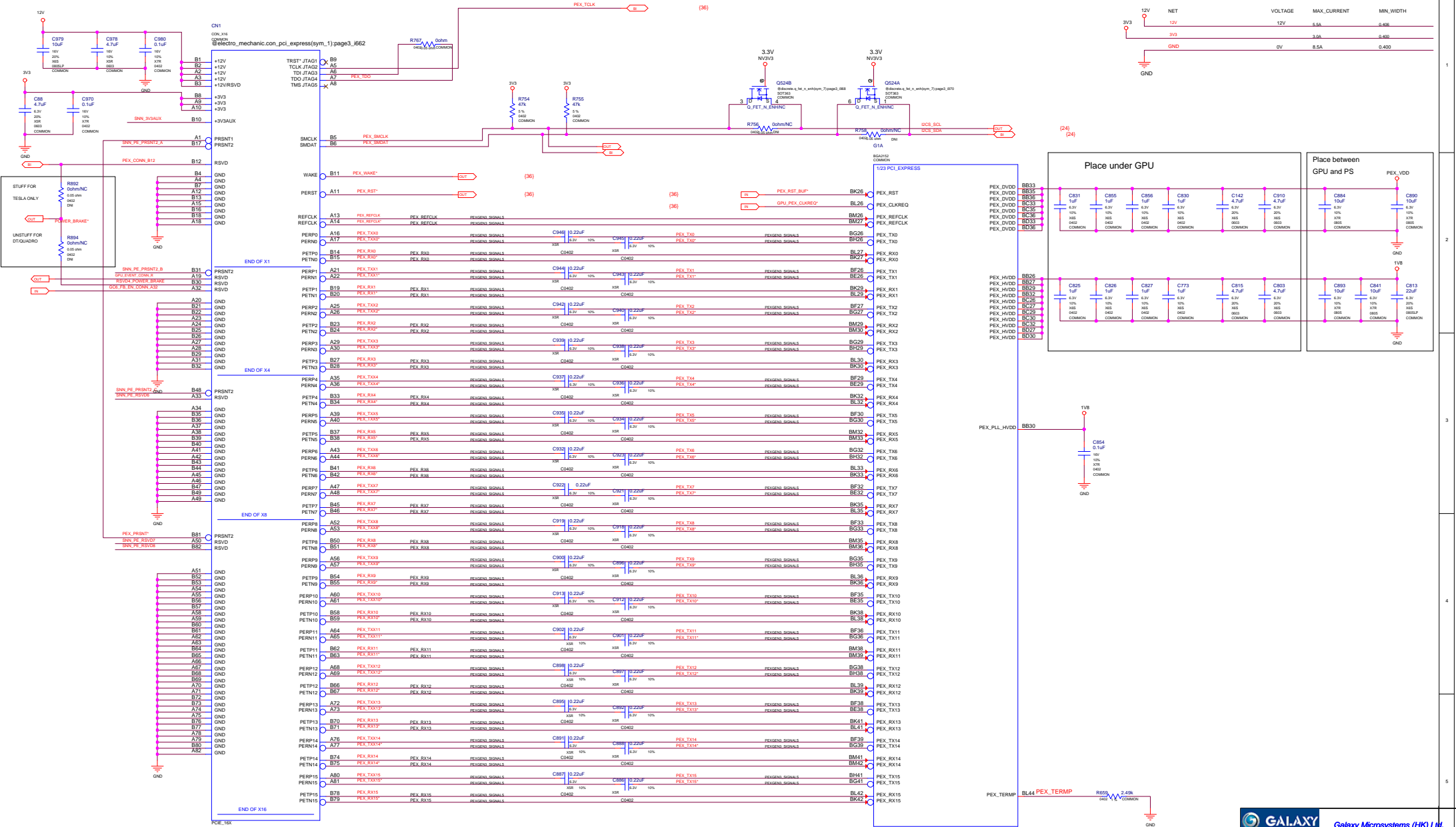
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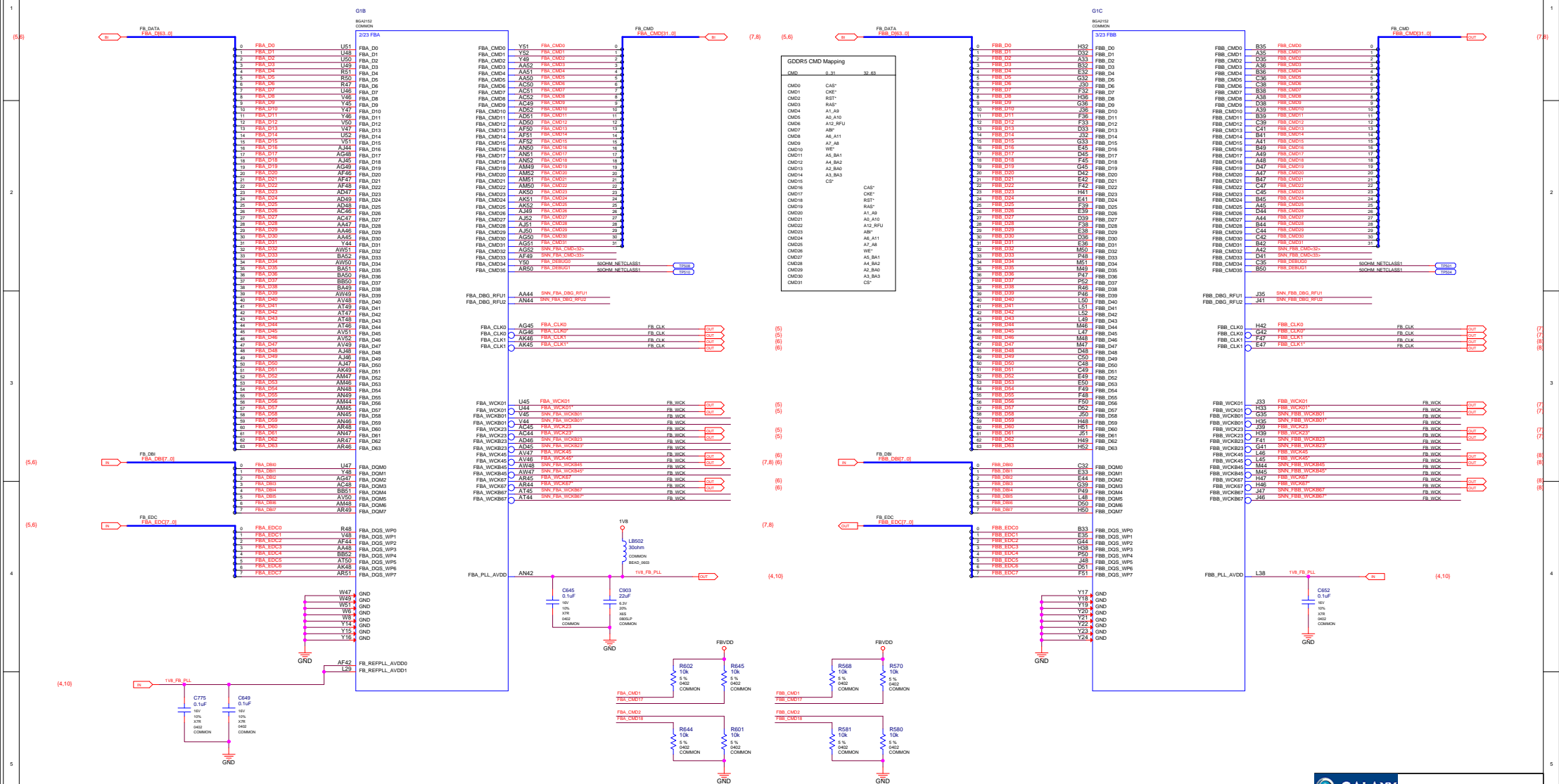
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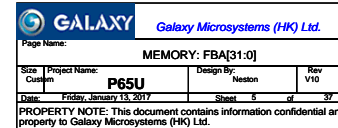
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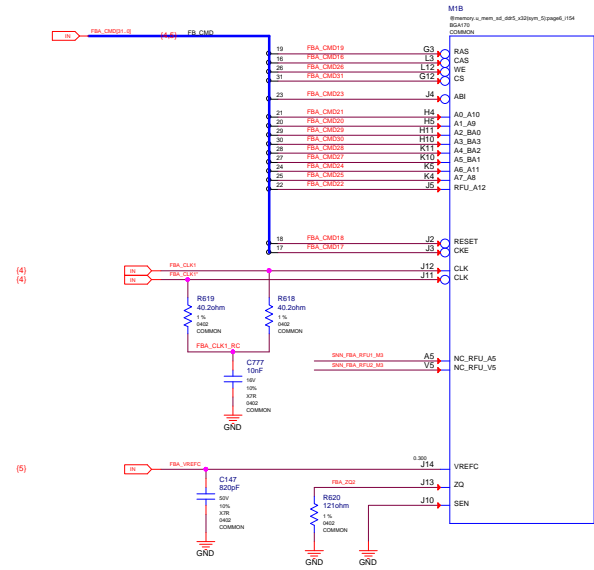
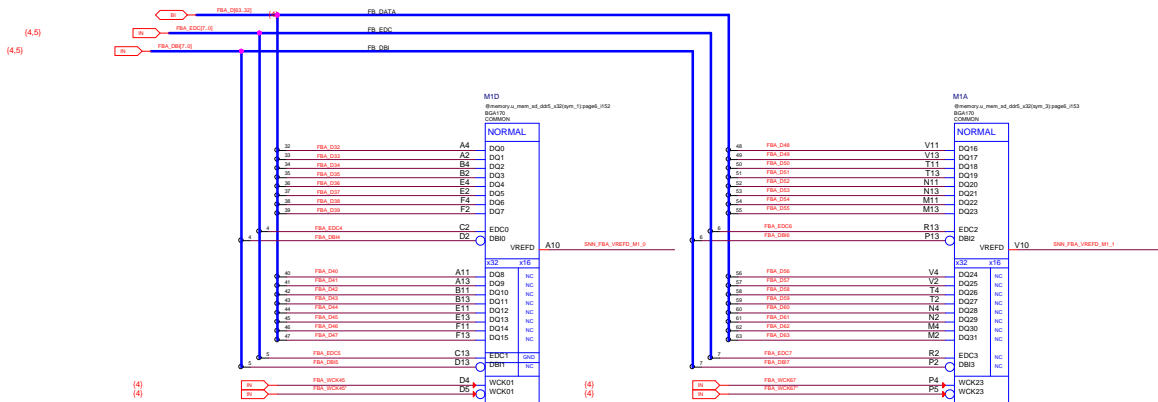
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Rev

V10

Date:

Friday, January 13, 2017

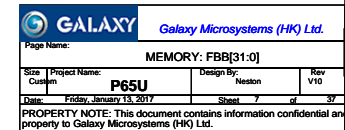
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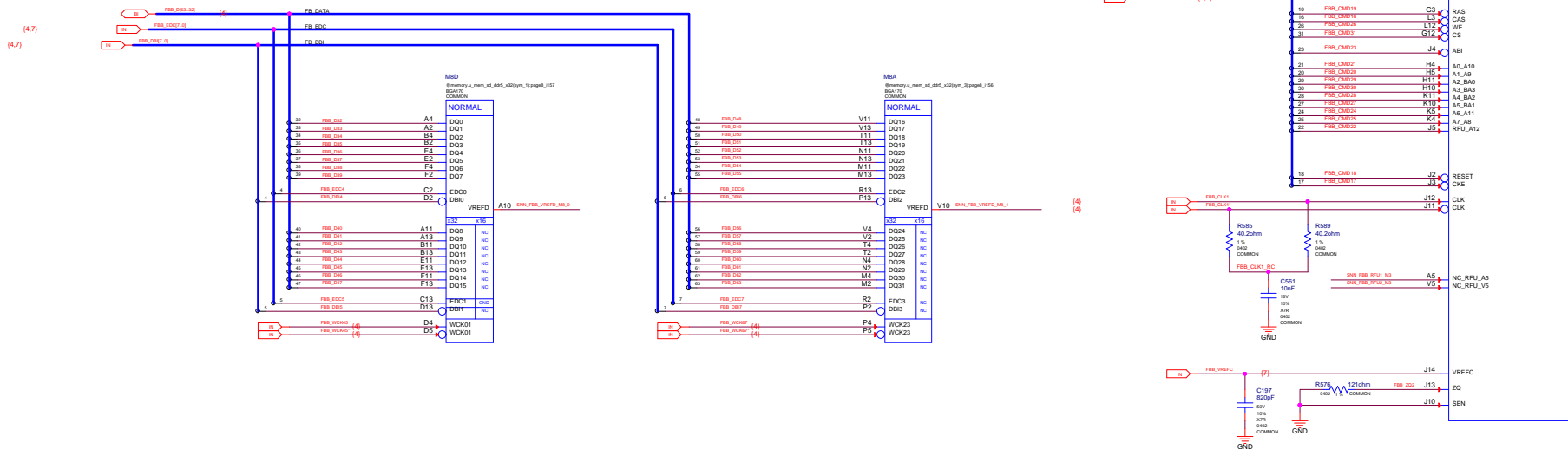
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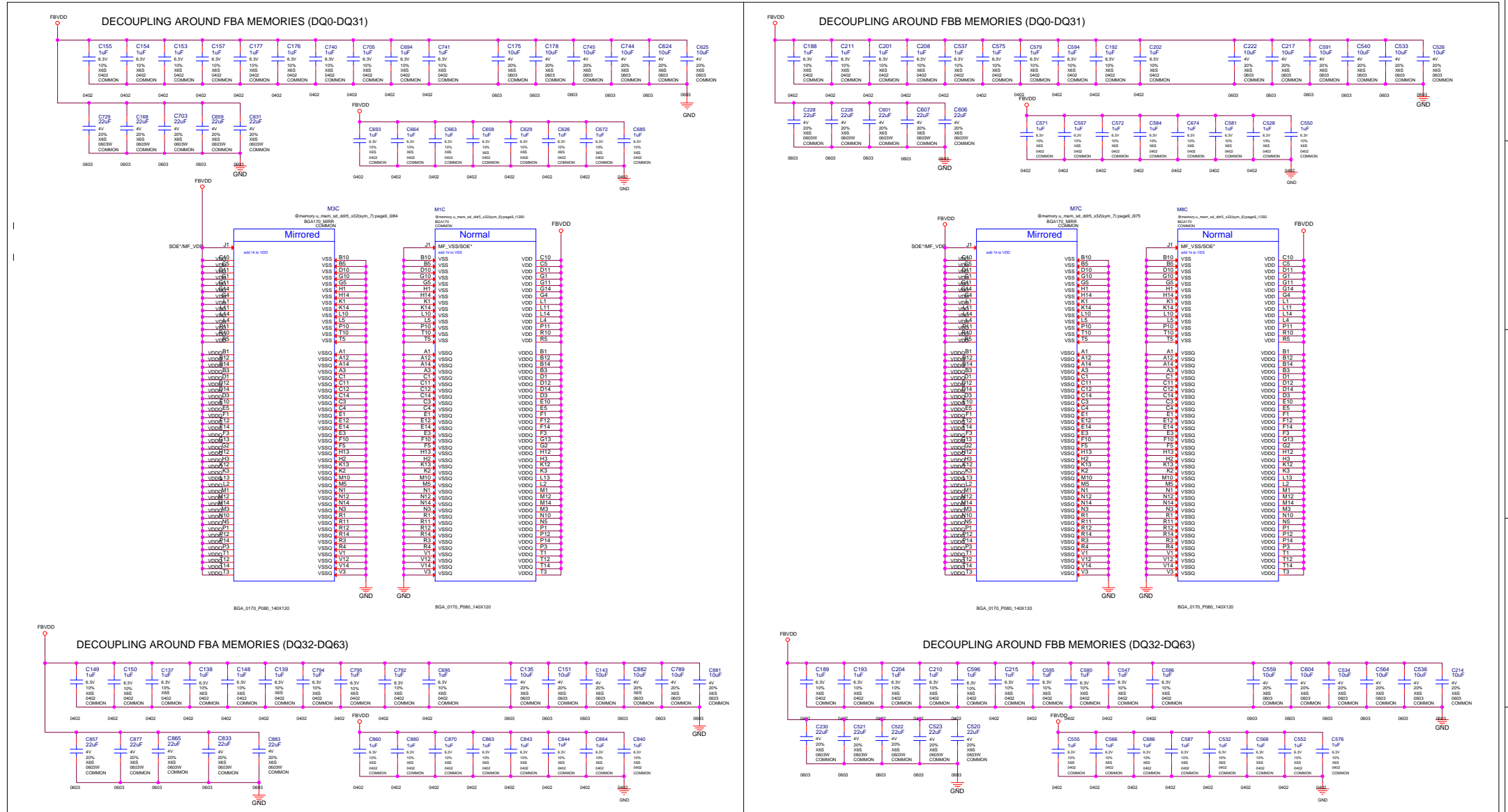


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MEM FR\_AB\_PWR

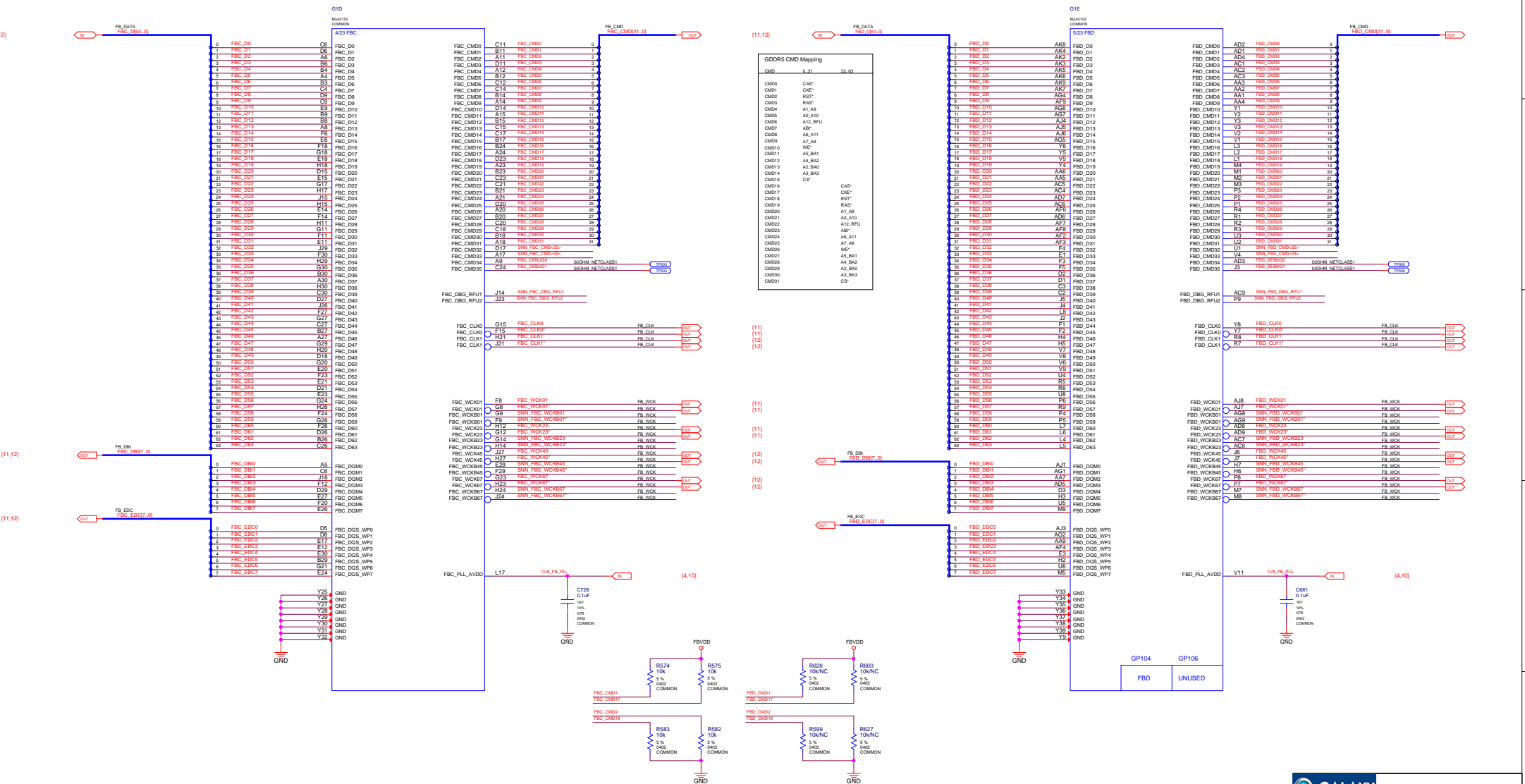
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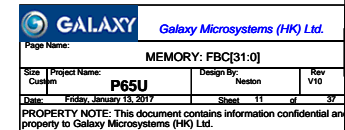
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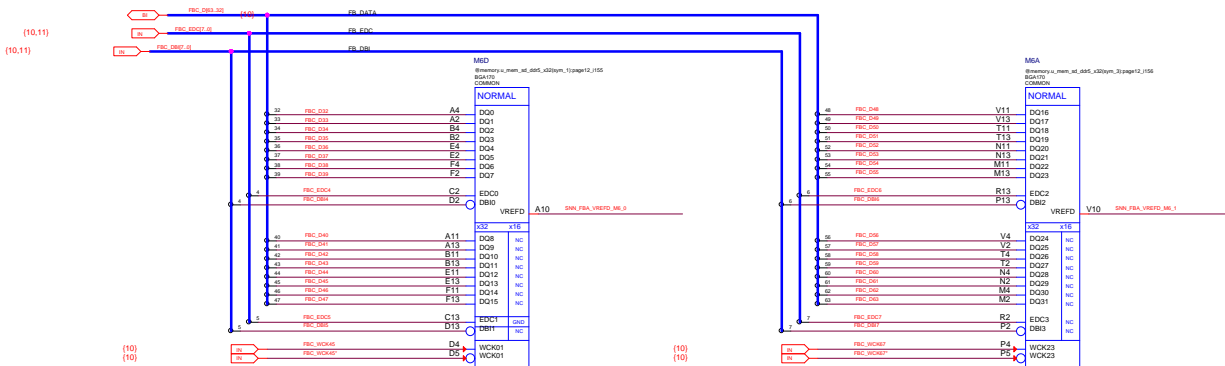
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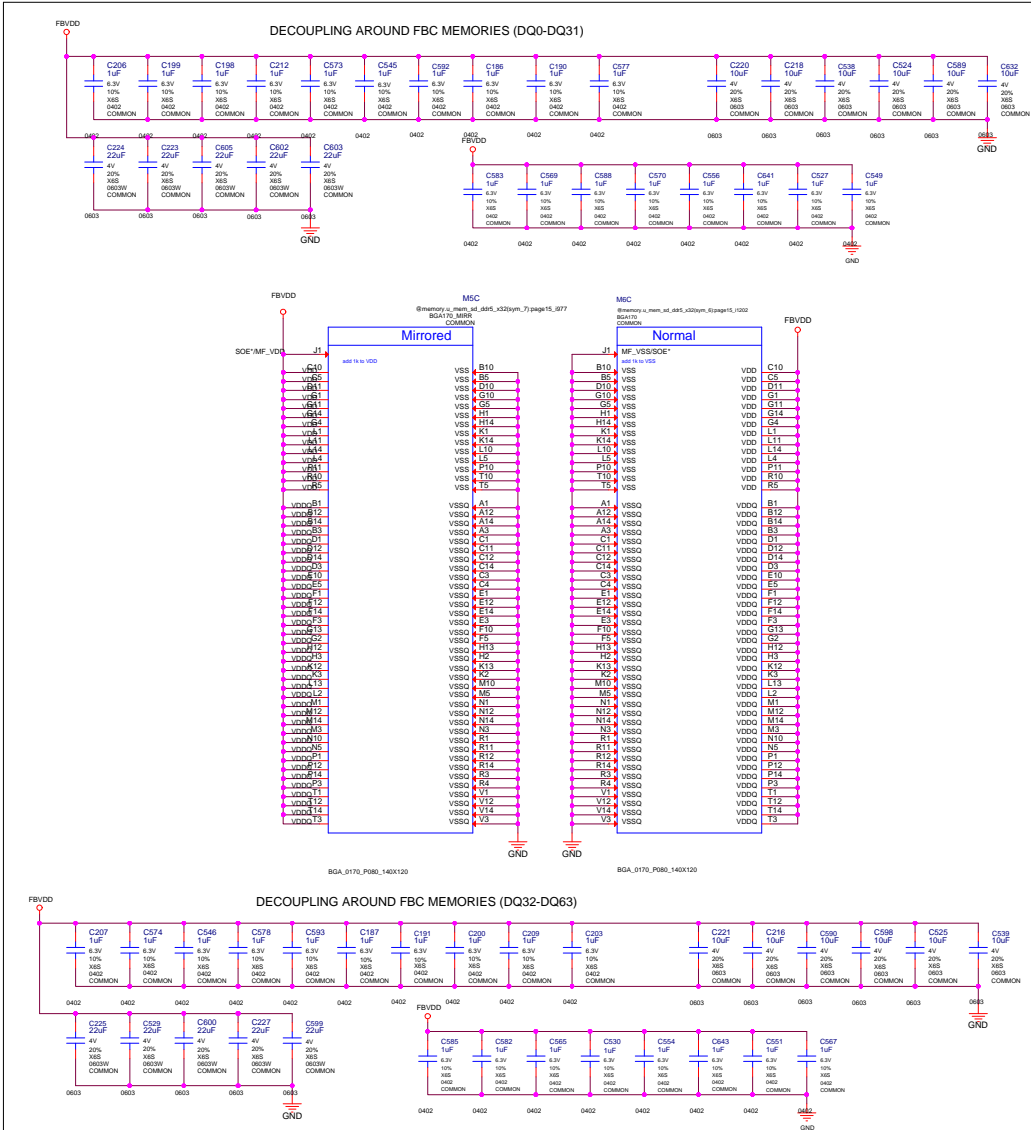
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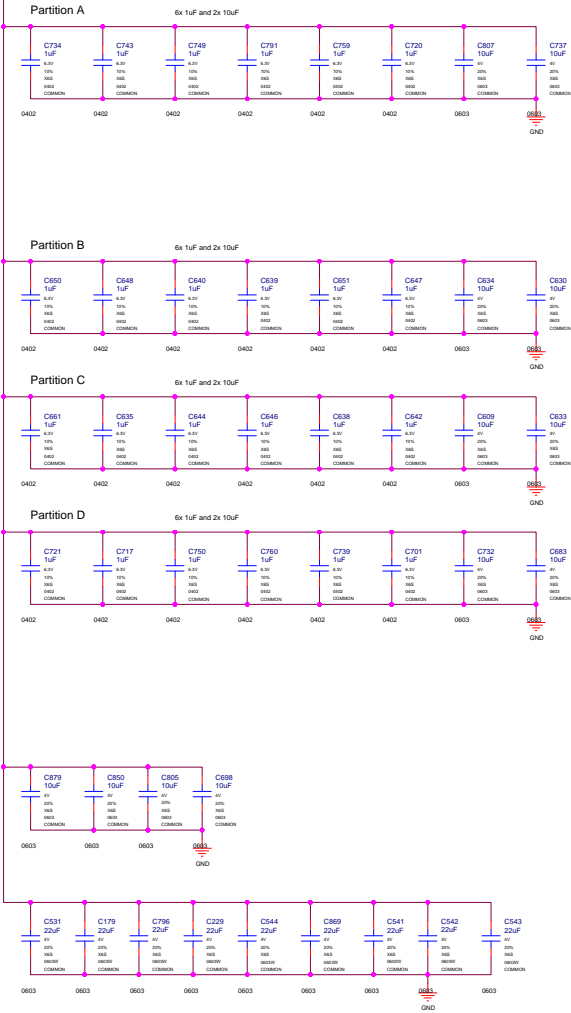




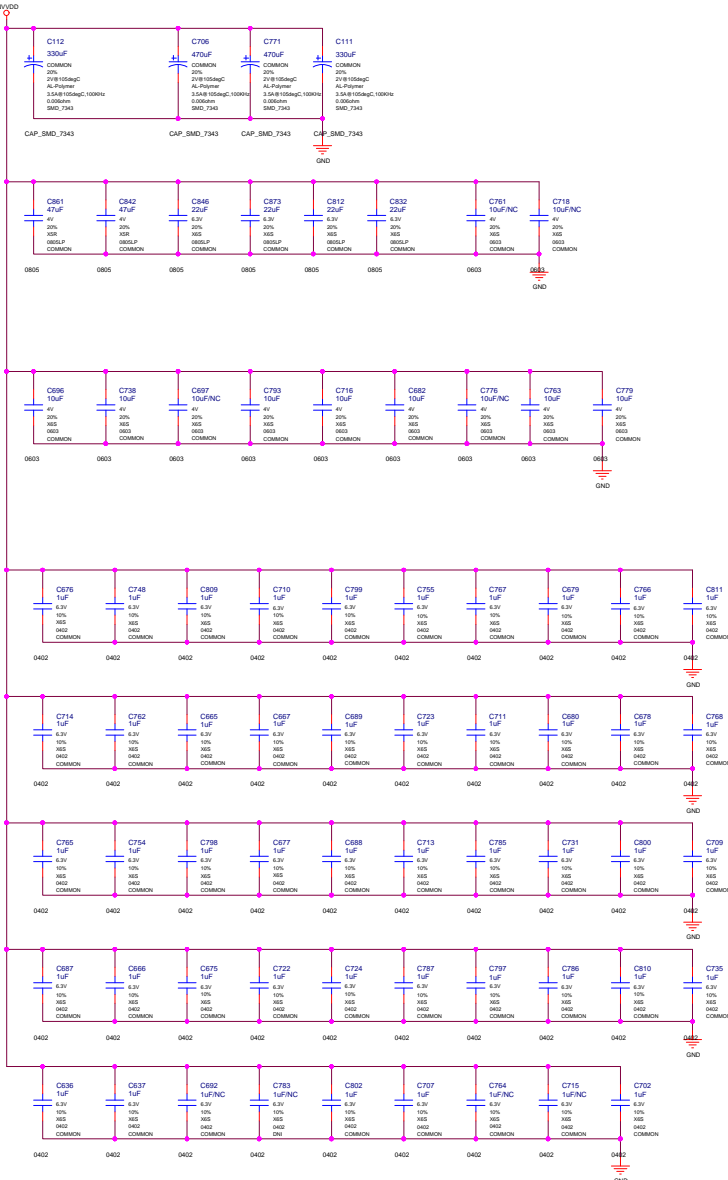




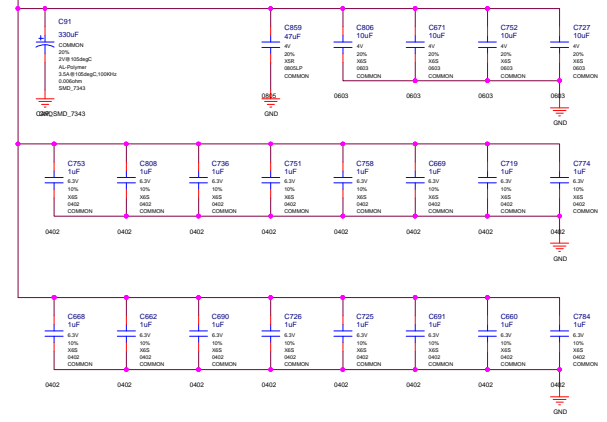
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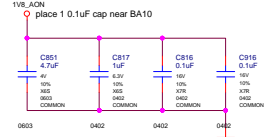
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NVDD

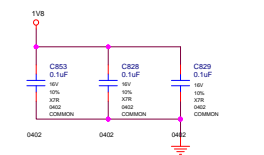


1V8\_AON



place 1.0.1uF cap for BB14 and BC14 to share

1V8\_MAIN



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ASSEMBLY PAGE DETAIL  
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GPU Decoupling

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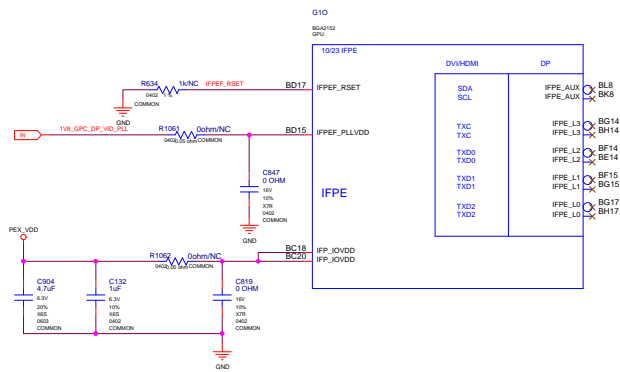
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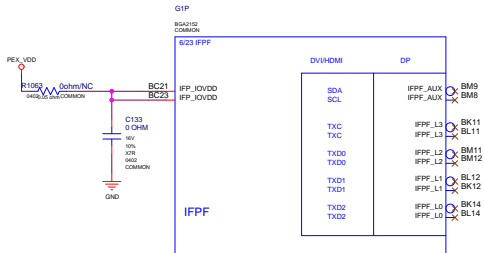




ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	IFPE DP


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Size	Project Name:	Design By:	Rev
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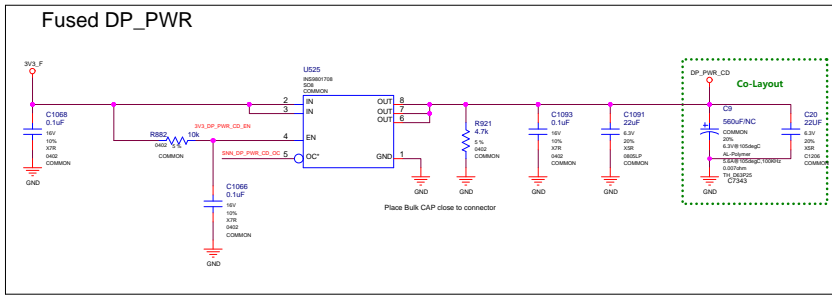
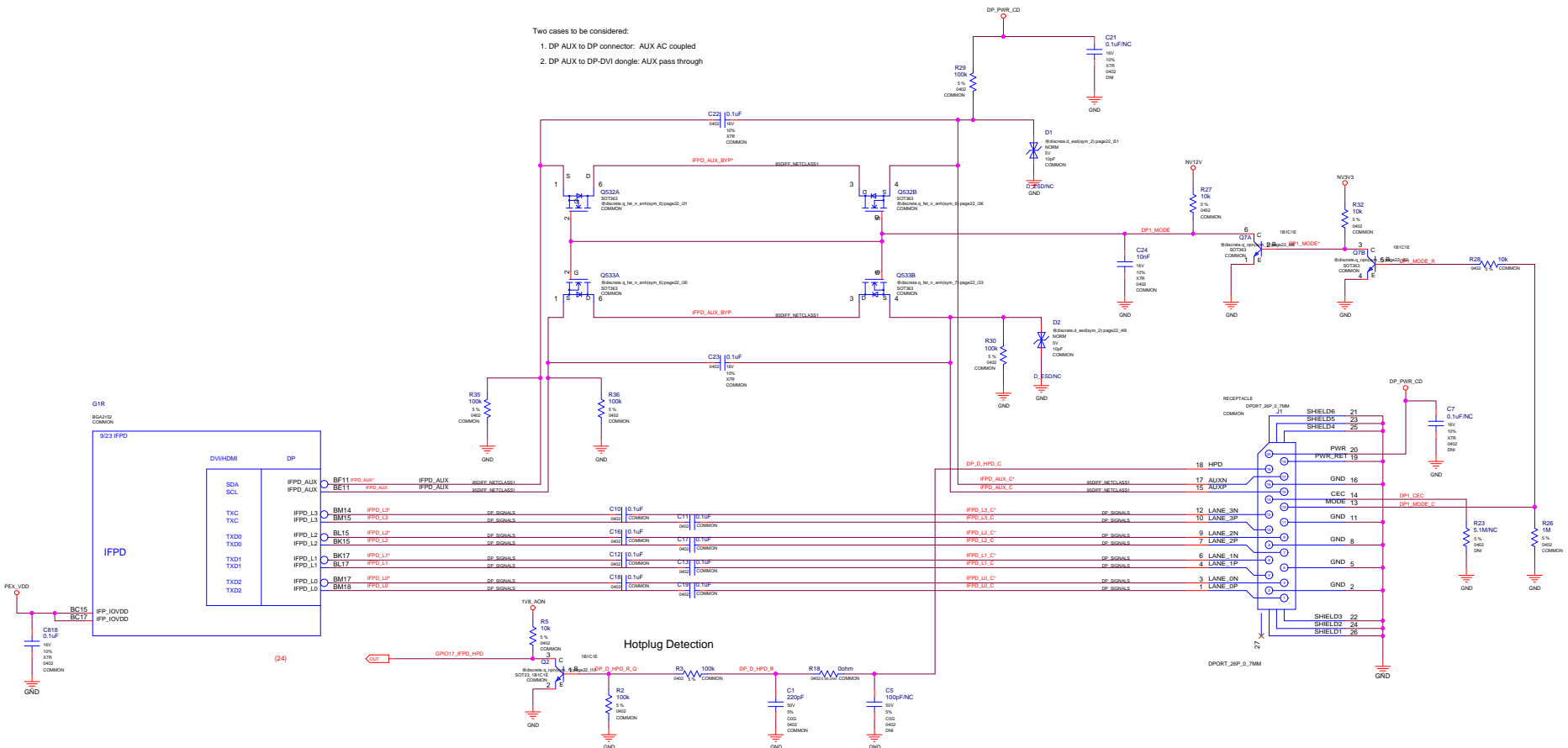
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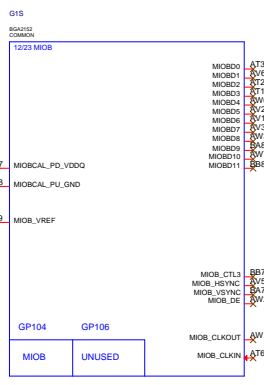
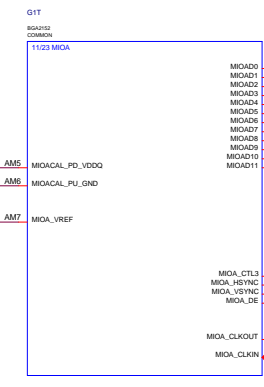
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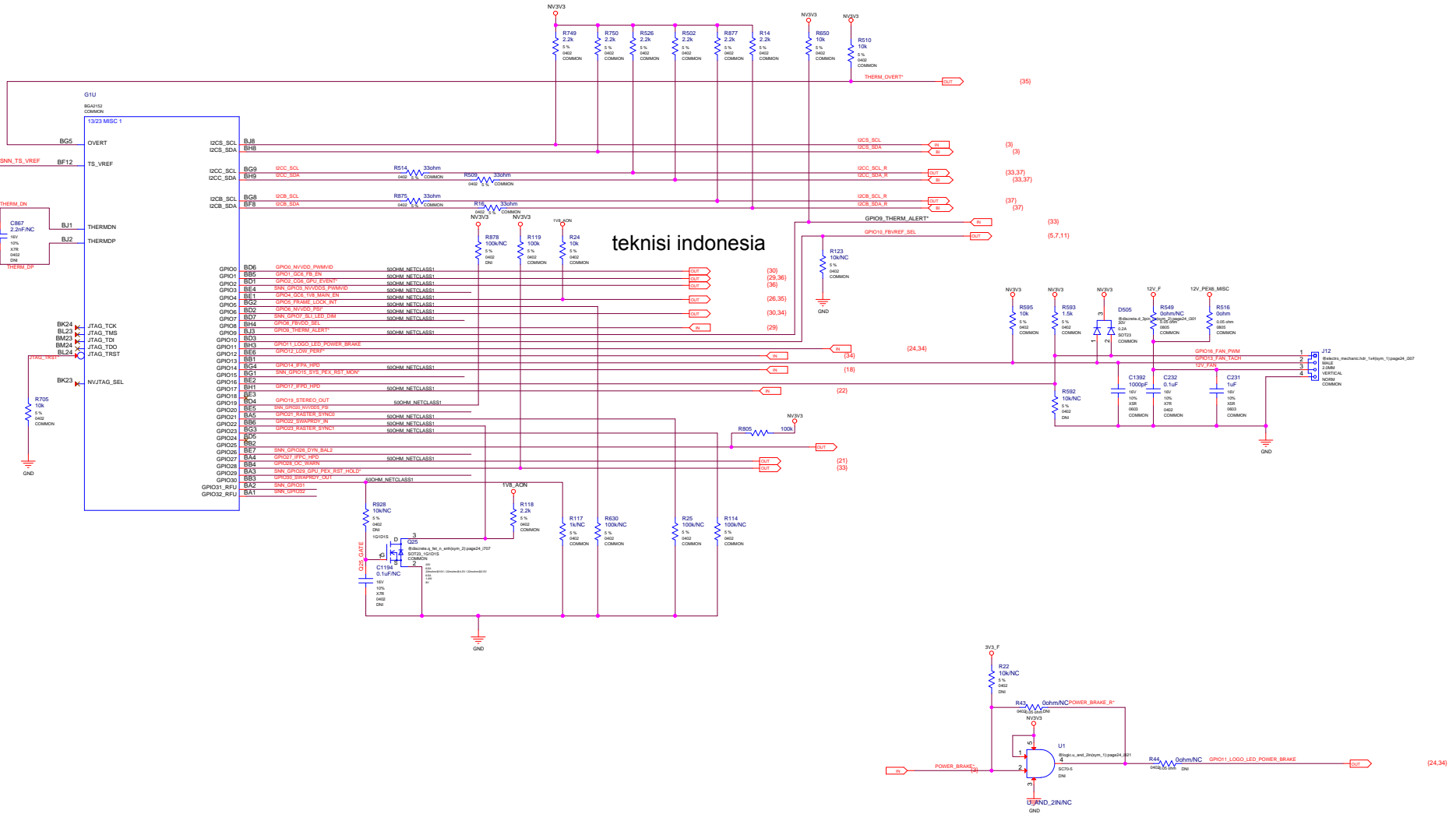
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ASSEMBLY PAGE DETAIL	«ASSEMBLY_DESCRIPTION» MIOA/B Interface and Frame Lock
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO, STEREO

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Page Name: MISC1: Fan, Thermal, JTAG, GPIO, STEREO

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	H	1110	SOR0/1/2/3 ENABLE
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

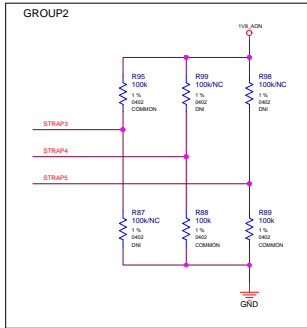
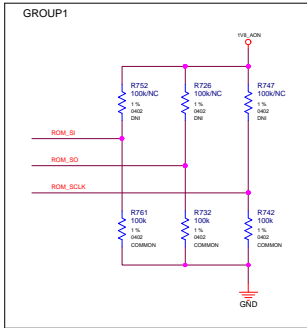
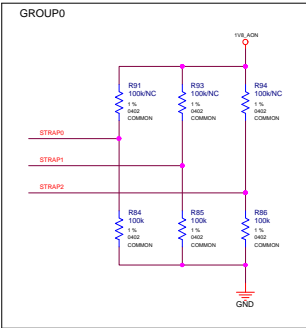
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

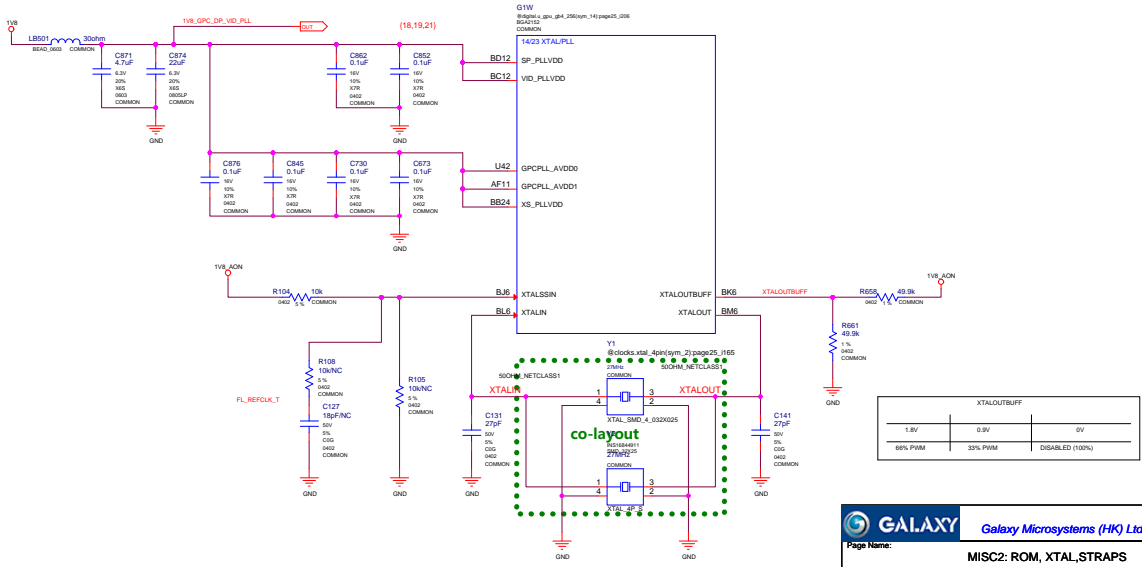
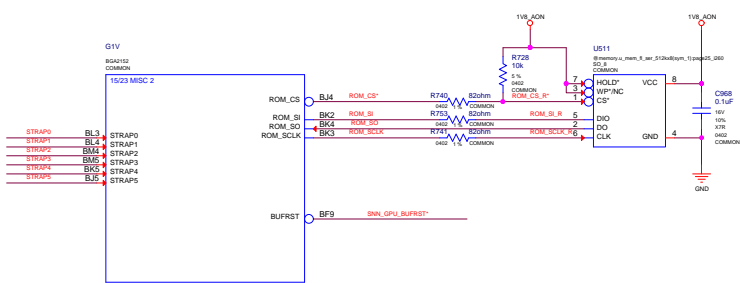
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

ASSEMBLY  
PAGE DETAIL

ASSEMBLY DESCRIPTION  
MISC2: ROM, XTAL,STRAPS



CFG(3:0)	Config	Width	Vendor
0000	256Mx32	256-bit	Samsung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



XTALOUTBUFF		
1.5V	0.9V	0V
85% PWM	33% PWM	DISABLED (100%)

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MISC2: ROM, XTAL,STRAPS

Size | Project Name: P65U | Design By: Neston | Rev: V10

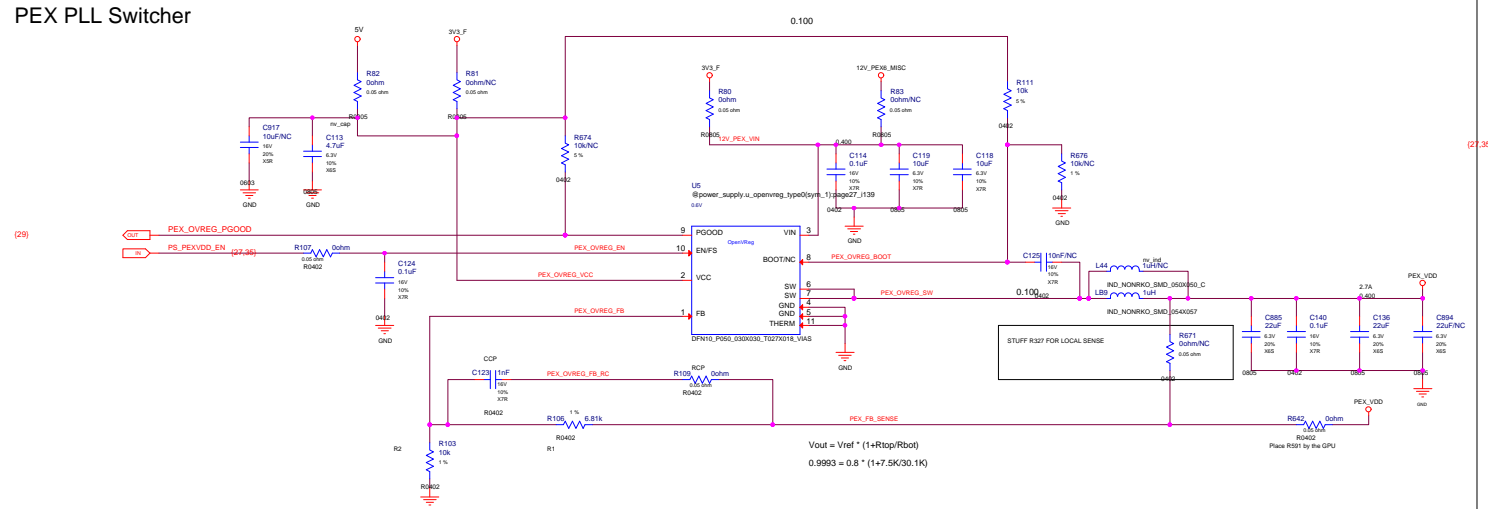
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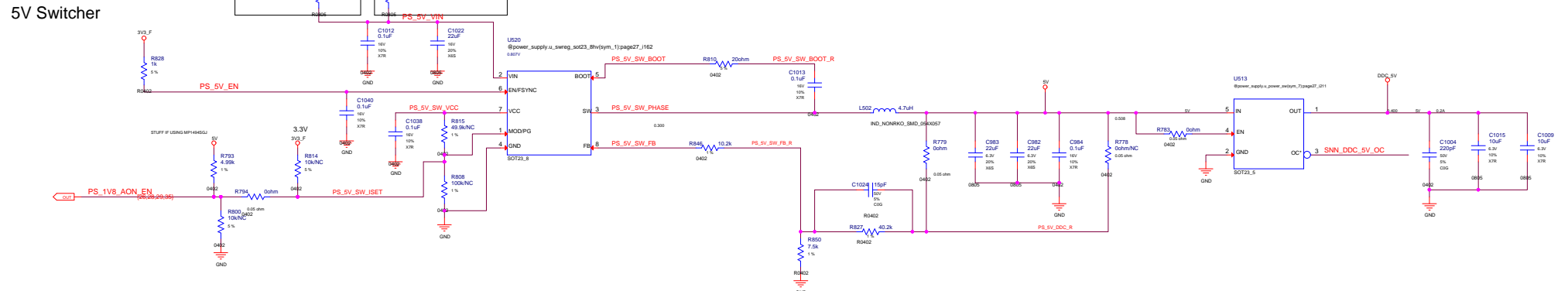




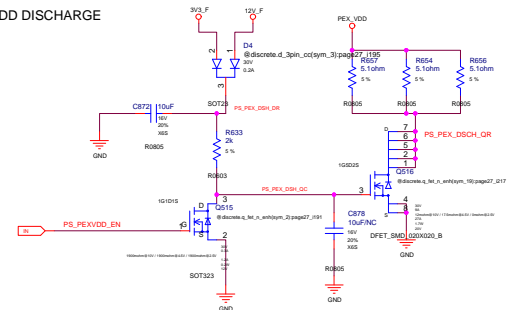
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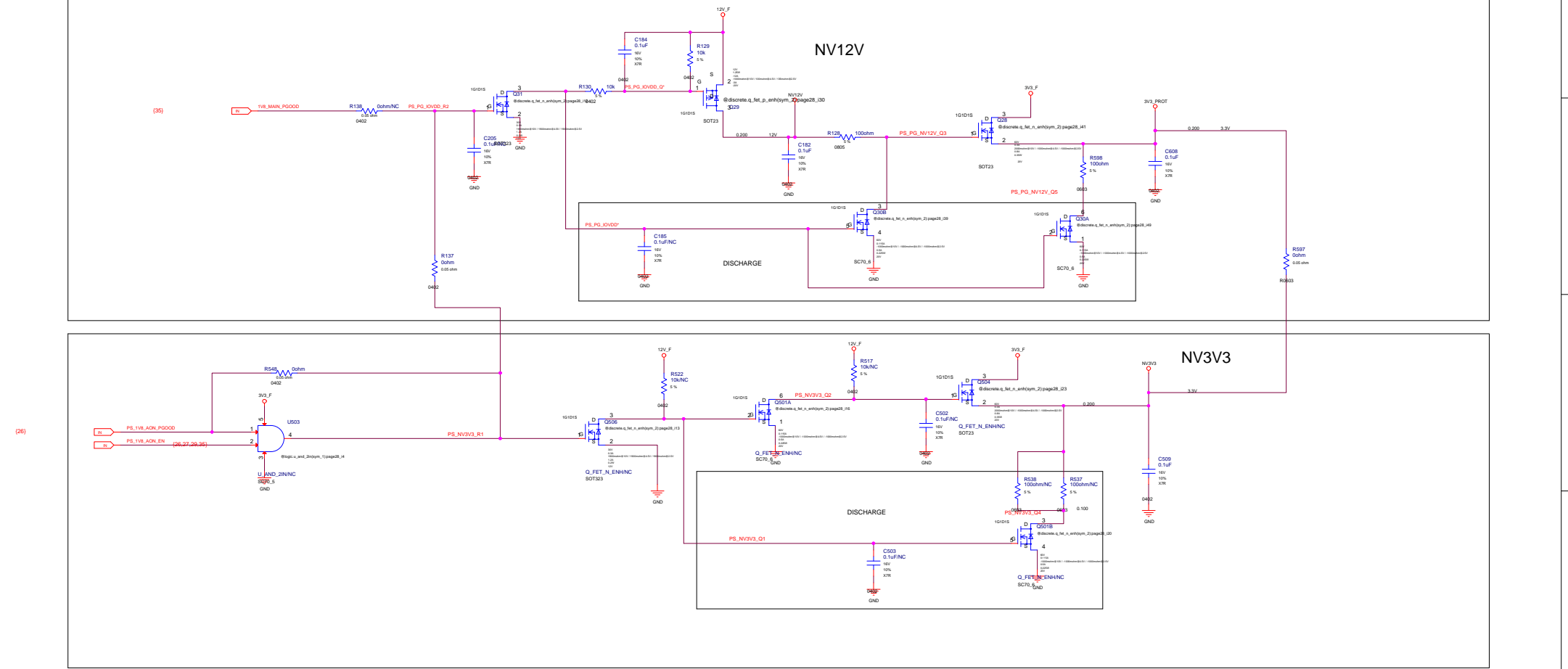


## 5V Switcher




## PEX\_VDD DISCHARGE





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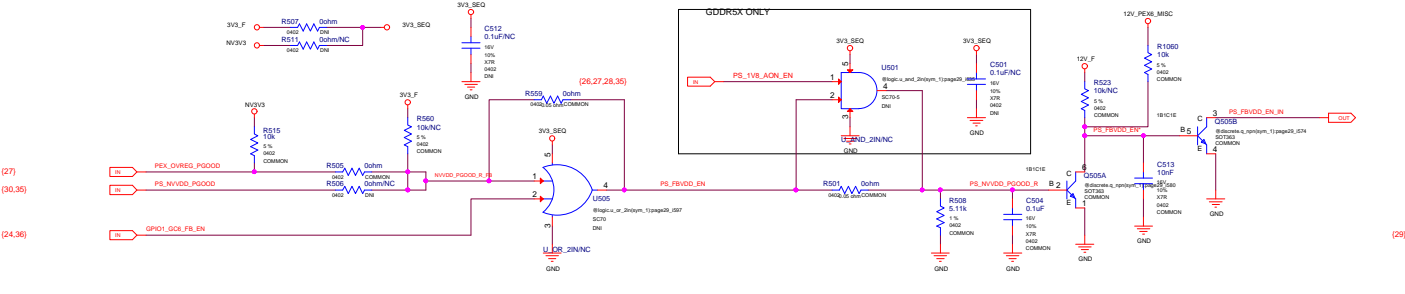
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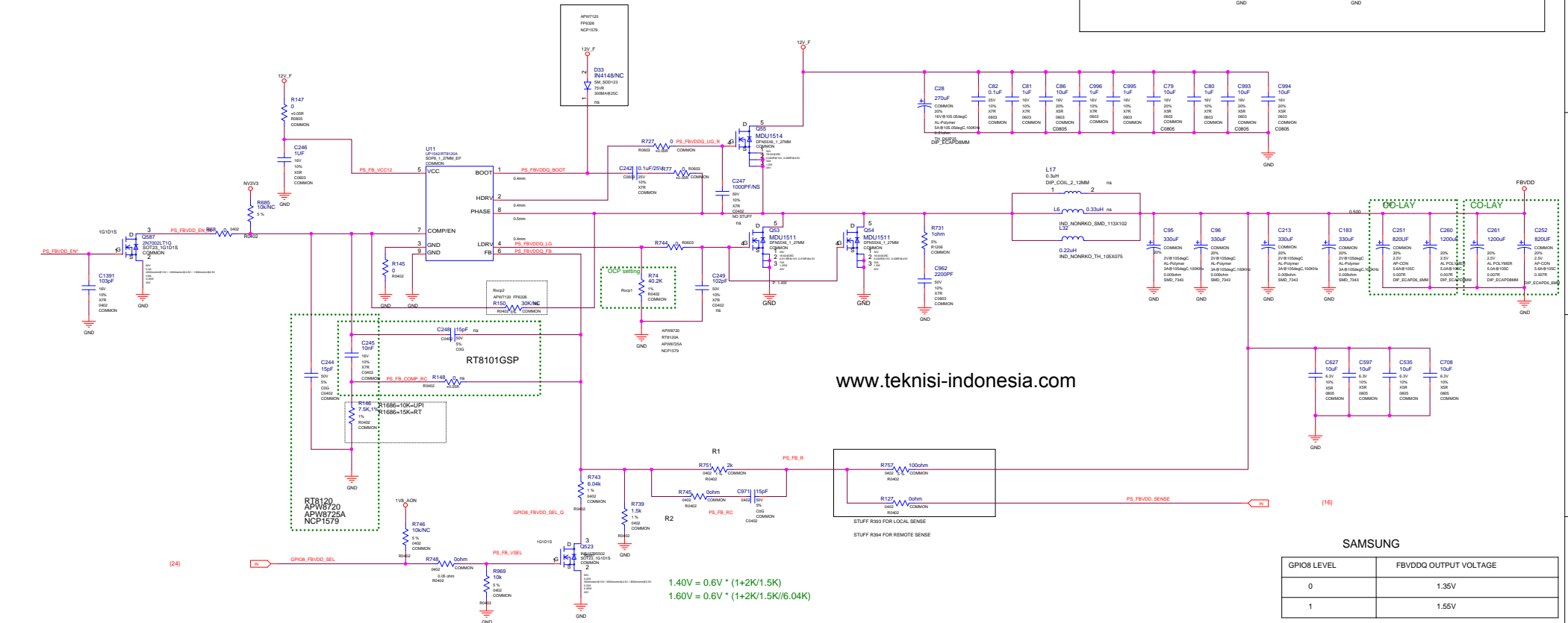
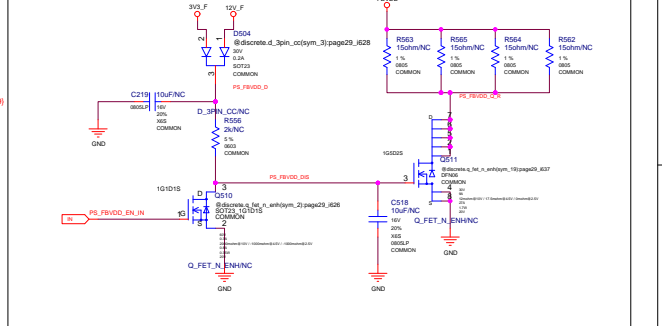
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### FBVDD/Q Enable



### FBVDD DISCHARGE



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### SAMSUNG

GPIO8 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.35V
1	1.55V

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Page Name: PS: FBVDD

Size: Project Name: P65U Design By: Neston Rev: V10

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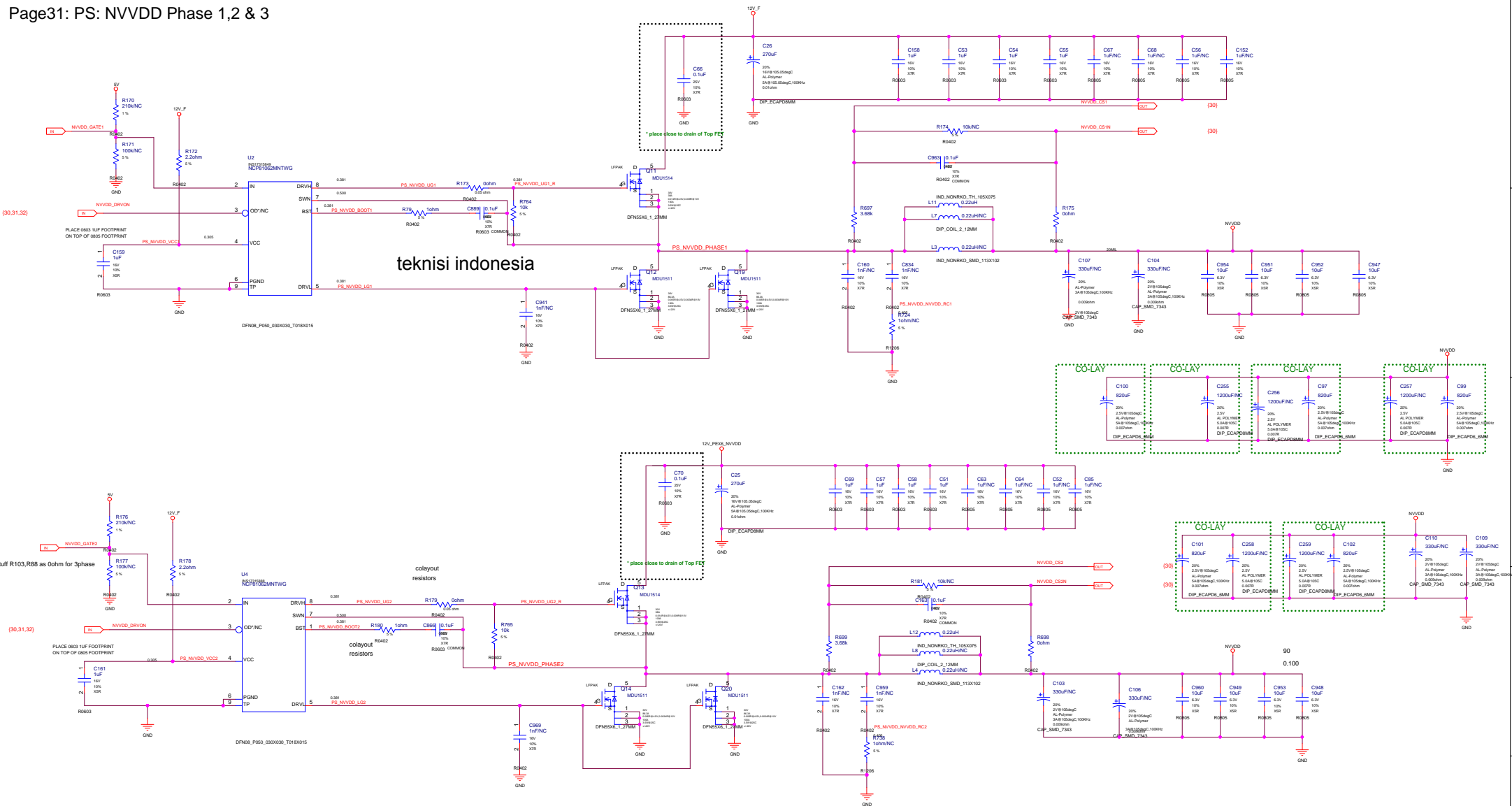
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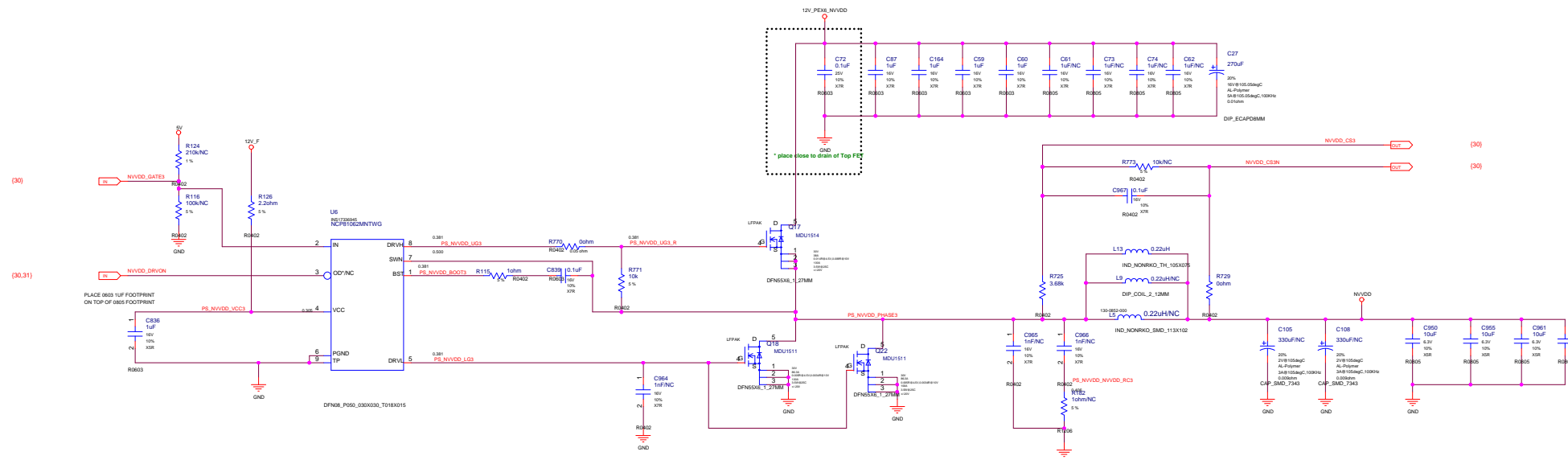
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ASSEMBLY PAGE DETAIL

ASSEMBLY DESCRIPTION: PS: FBVDDQ







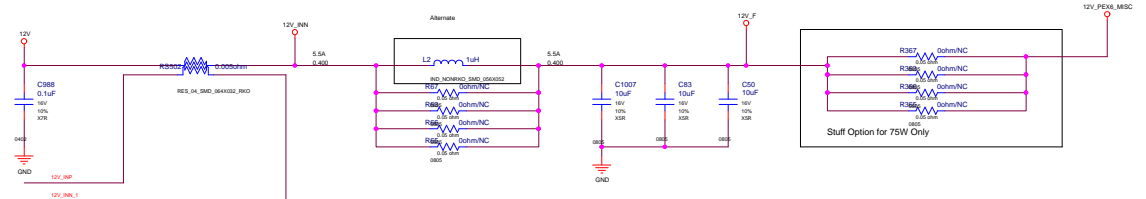
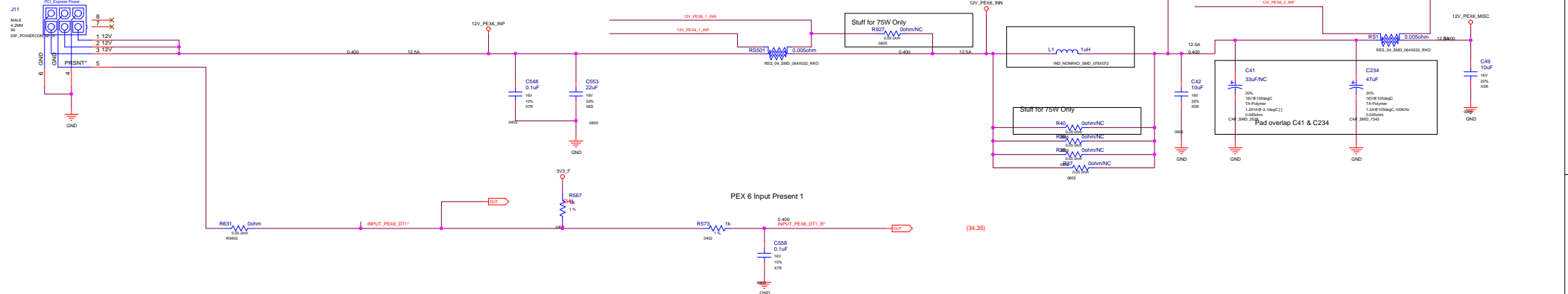
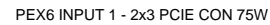
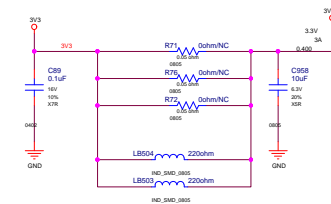
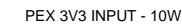
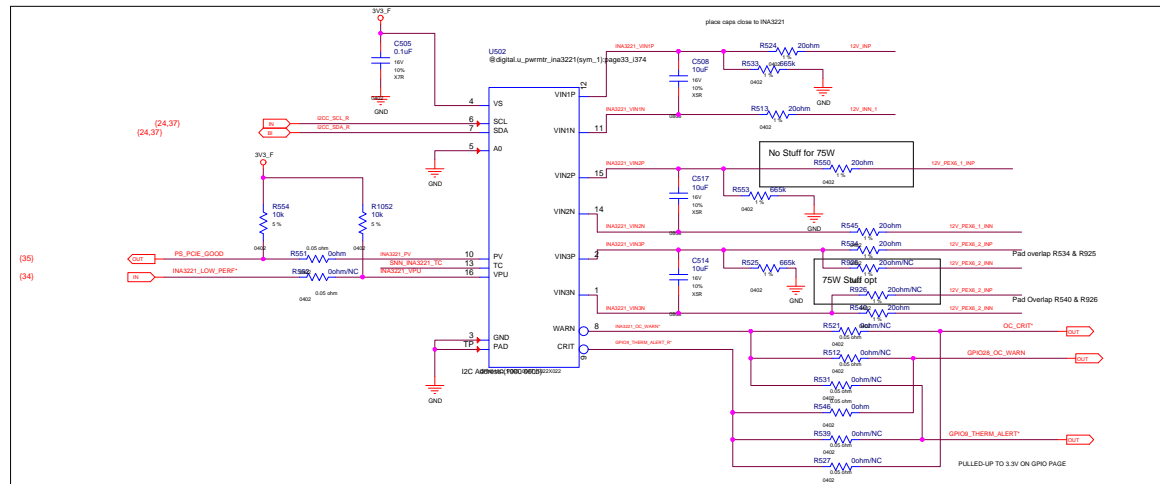
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ASSEMBLY	ASSEMBLY_DESCRIPTION
PAGE DETAIL	PS: NVVDD Rail Balance Logic & Dynamic Phase

Page Name:  
**PS: NVVDD Rail Balance Logic & Dynamic Phase**

Size	Project Name:	Design By:	Rev
Cuclen	<b>P65U</b>	Neston	V10
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Place close to J14/J16  
J14 and J16 is the soldering holes for power cable.  
The power cable Need a separete wire as detect pin  
This detect wire need be soldered on J15

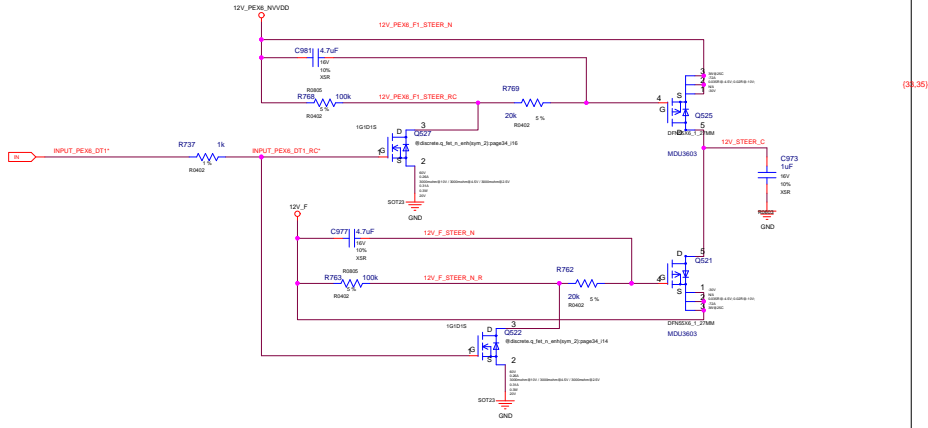
ASSEMBLY PAGE DETAIL	«ASSEMBLY_DESCRIPTION» PS: Input, Filtering, and Monitoring
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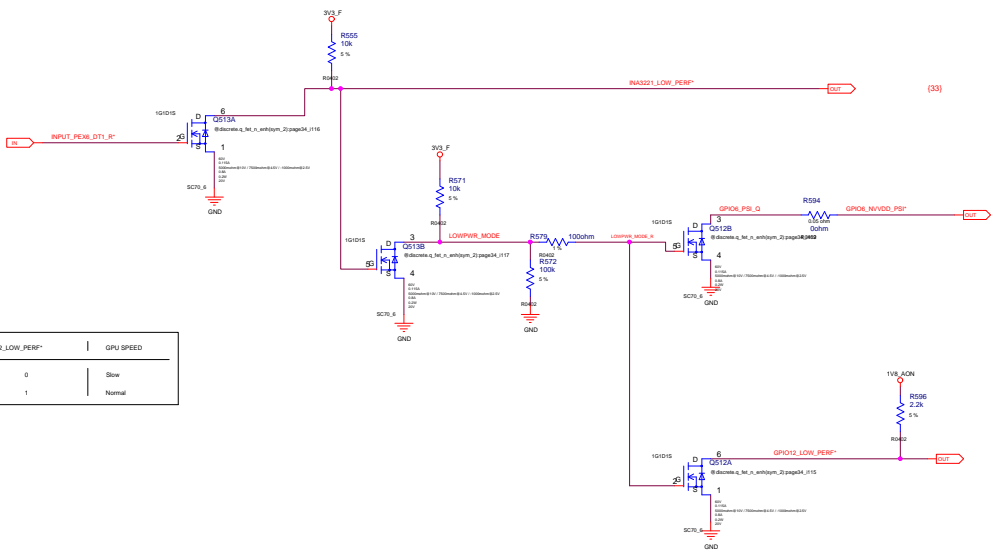
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Page Name:			
<b>PS: Input, Filtering, and Monitoring</b>			
Size	Project Name:	Design By:	Rev
Customer		Neston	V10
<b>P65U</b>			
Date:	Friday, January 13, 2017	Sheet	33 of 37
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12V CURRENT STEERING (UNDER POWER BOOT):

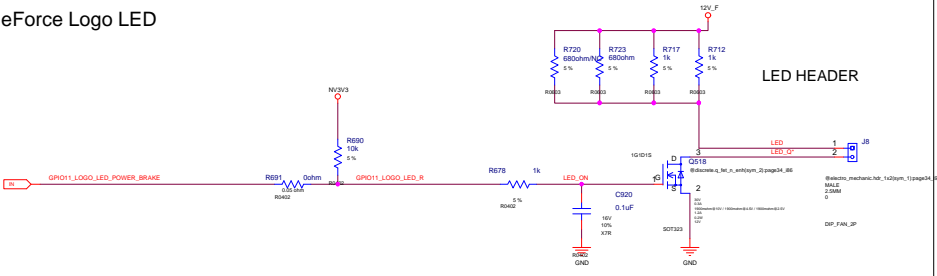
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI\* Control



GeForce Logo LED



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ASSEMBLY PAGE DETAIL  
PS: 12V Power Steering, PSI Control & LED

Page Name: PS: 12V Power Steering, PSI Control & LED

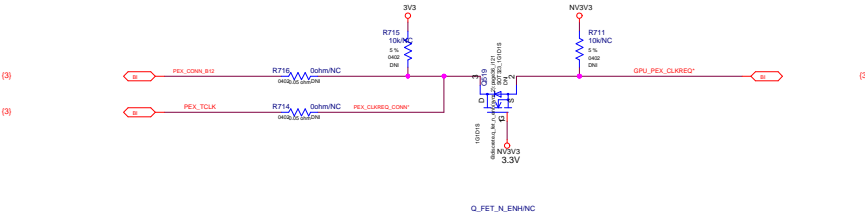
Size	Project Name: P65U	Design By: Neston	Rev: V10
Date: Friday, January 13, 2017	Sheet: M	4	37

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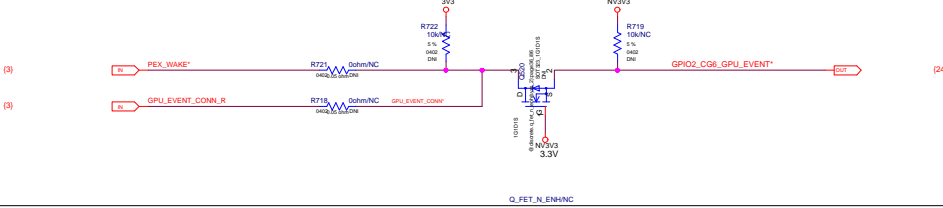




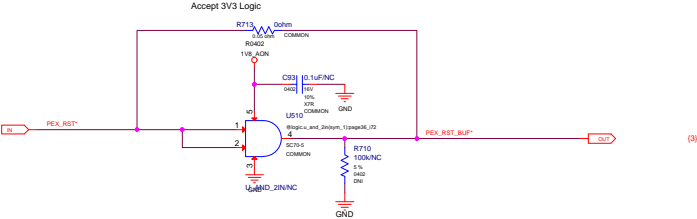
PEX\_CLKREQ\*



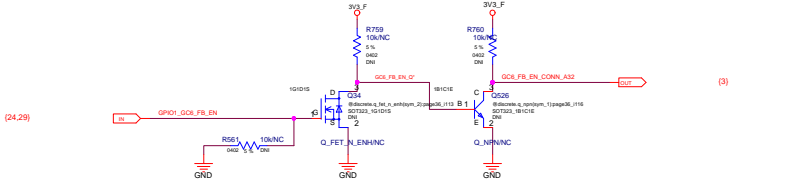
GPU\_EVENT\*



PEX\_RST# LOGIC



GC6 FB ENABLE



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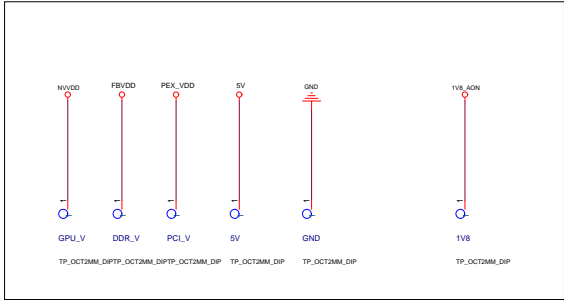
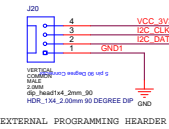
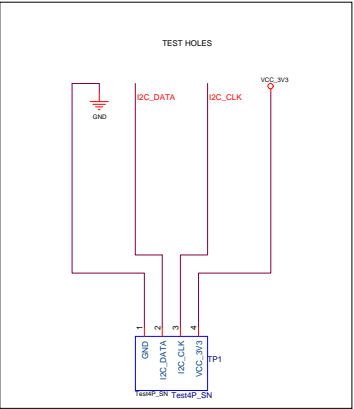
ASSEMBLY PAGE DETAIL	ASSEMBLY DESCRIPTION PS: GC6 MISC
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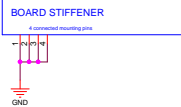
Page Name: PS: GC6 MISC			
Size: A4	Project Name: P65U	Design By: Neston	Rev: V10
Date: Friday, January 13, 2017	Sheet: 38	4	37

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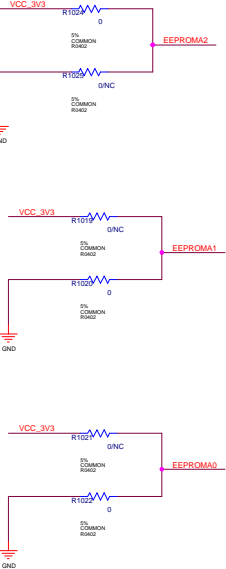
37\_MECH\_SN EEPRON



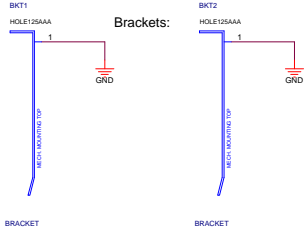
GPU Stiffener:



MOUNTING HOLES FOR HS DS:



Brackets:




MOUNTING HOLES FOR HS SS:

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MECH

 <b>GALAXY</b>		<b>Galaxy Microsystems (HK) Ltd.</b>	
Page Name: <b>MECH_SN EEPRON</b>			
Size Custom	Project Name: <b>P65U</b>	Design By: Neston	Rev V10
Date: Friday, January 13, 2017		Sheet 37	of 37
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